WHAT IS CLAIMED IS:

1. A voltage amplifier, comprising:

an amplifier stage to amplify an input signal;

a bias current generator to supply a bias current to the amplifier stage, the bias current generator controllable in response to a frame rate signal, the frame rate signal being representative of a video frame rate; and

a compensation network to stabilize a loop response of the voltage amplifier, the compensation network controllable in response to the frame rate signal.

2. The voltage amplifier of Claim 1 wherein the compensation network includes a Miller compensator.

3. The voltage amplifier of Claim 2 wherein the Miller compensator includes a controlled capacitor having a value responsive to the frame rate signal.

4. The voltage amplifier of Claim 3 wherein the Miller compensator further includes a controlled resistor having a value responsive to the frame rate signal.

5. The voltage amplifier of Claim 4 wherein the controlled resistor includes a Field Effect Transistor operated in the active region.

6. The voltage amplifier of Claim 4 wherein the controlled resistor includes a first combination of a first switch and a compensation resistor; and

the controlled capacitor includes a second combination of a second switch and a compensation capacitor.

7. The voltage amplifier of Claim 1 wherein the amplifier stage includes a first stage and a second stage.

8. The voltage amplifier of Claim 7 wherein the compensation network is coupled between the first stage and the second stage.

9. A voltage amplifier having a controlled output comprising:

a first stage to amplify an input signal;

a second stage coupled to an output of the first stage to generate the controlled output.

a first bias current generator to supply a first bias current to the first stage, the first bias current generator controllable in response to a frame rate signal;

a second bias current generator to supply a second bias current to the second stage, the second bias current generator controllable in response to the frame rate signal; and

a compensation network coupled between the first stage and the second stage to stabilize a loop response of the voltage amplifier, the compensation network controllable in response to the frame rate signal.

10. The voltage amplifier of Claim 9 wherein the compensation network includes a controlled capacitor having a value responsive to the frame rate signal.

11. The voltage amplifier of Claim 10 wherein the compensation network further includes a controlled resistor having a value responsive to the frame rate signal.

12. The voltage amplifier of Claim 4 wherein the controlled resistor includes a Field Effect Transistor operated in the active region.

13. The voltage amplifier of Claim 11 wherein the controlled resistor includes a first combination of a first switch and a compensation resistor; and

the controlled capacitor includes a second combination of a second switch and a compensation capacitor.

14. A CMOS imager, comprising:

an array of CMOS active pixel sensors;

a row driver circuit to select a row of sensors in the array;

a column readout circuit to readout a column of sensors in the array;

a timing and control circuit to control the row driver circuit and the column readout circuit; and

a voltage amplifier, in response to an input signal, to generate a voltage signal, the voltage amplifier including;

an amplifier stage to amplify an input signal;

a bias current generator to supply a bias current to the amplifier stage, the bias current generator controllable in response to a frame rate signal; and

a compensation network to stabilize a loop response of the voltage amplifier, the compensation

network controllable in response to the frame rate signal.

15. The CMOS imager of Claim 14 wherein the compensation network includes a Miller compensator.

16. The voltage amplifier of Claim 15 wherein the Miller compensator includes a controlled capacitor having a value responsive to the frame rate signal.

17. The voltage amplifier of Claim 16 wherein the Miller compensator further includes a controlled resistor having a value responsive to the frame rate signal.

18. The voltage amplifier of Claim 17 wherein the controlled resistor includes a Field Effect Transistor operated in the active region.

19. The voltage amplifier of Claim 17 wherein the controlled resistor includes a first combination of a first switch and a compensation resistor; and

the controlled capacitor includes a second combination of a second switch and a compensation capacitor.

20. A method of generating a driver voltage for a CMOS imager, comprising:

providing an amplifier including a compensation network;

determining a video frame rate of the CMOS imager;

in the amplifier, generating the driver voltage as a function of an input voltage;

controlling a bias current of the amplifier as a function of the video frame rate such that at a lower frame rate the bias current is reduced; and

controlling a capacitance of the compensation network as a function of the video frame rate such that at a lower frame rate a bandwidth of the amplifier is reduced.

21. The method of Claim 20 further comprising controlling a resistance of the compensation network as a function of the video frame rate such that a predetermined phase margin of the amplifier is maintained for a range of frame rates.